

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Applicant	:	V. K. JaiPrakash, et al.)	Examiner:
)	TBA
Serial No.	:	TBA)	
)	
Filed	:	Filed Herewith)	Art Unit
)	Unknown
For	:	DRAM VERTICAL TRANSISTOR AND)	
		TRENCHCAPACITOR MEMORY CELLS)	
		AND METHOD OF FABRICATION)	

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner For Patents
P. O. Box 1450
Alexandria, VA 22313-1450

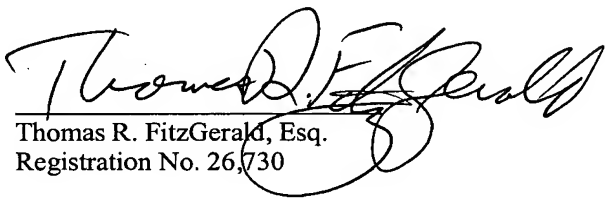
Dear Sir:

Pursuant to 37 CFR §1.97 - §1.98, Applicants hereby bring to the attention of the United States Patent and Trademark Office, the references listed on the attached Form PTO-1449. Copies are not included because the cited references were cited by the USPTO in the parent application identified on page 1 of the specification.

Respectfully submitted,

Date

7/11/03


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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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